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Intellectual Property Counselors

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Facsimile Transmission

TO LOURDES CRUZ
FAX 703-308-7722
PHONE
RE 10/065,016

FROM JOEL BAIR
PAGES 22 + Coversheet
DATE 8 APRIL 2003

~~2841~~

☒ Urgent ☐ For Review ☐ Please Comment ☐ Please Reply ☐ Please Recycle

Comments:

MS. CRUZ:

FOR YOUR DISCUSSION WITH MS. CUNEO IN THE EVENT THE MAILROOM HAS NOT YET GOTTEN THE DOCUMENTS TO THE FILE, I HAVE FAXED THE PETITION AND AMENDMENT AS FILED BY FAX ON 17 MARCH 2003.

JOEL E. BAIR
616-742-3573
jeb@mcgarrybair.com

********** -COMM. JOU_ - ********** DATE MAR-17-2003 *** TIME 15:27 *** P.01

MODE = MEMORY TRANSMISSION START=MAR-17 15:21 END=MAR-17 15:27

FILE NO.= 067

STN NO.	COMM.	ONE-TOUCH/ ABBR. NO.	STATION NAME/EMAIL ADDRESS/TELEPHONE NO.	PAGES	DURATION
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-McGarry Bair LLP -

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PTO/SB/21 (08-00)

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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/065,016
Filing Date	September 12, 2002
First Named Inventor	Olivier Boireau
Group Art Unit	
Examiner Name	Lourdes C. Cruz
Total Number of Pages In This Submission: 12.	Attorney Docket Number: 71522-2

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
- ☐ Fee Attached
- ☐ Amendment / Response
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☒ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Additional Enclosure(s) *(please identify below):*

Declaration in Support of Petition

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TECHNOLOGY CENTER 2800

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	McGARRY BAIR LLP Joel E. Bair, Reg. No. 33,356
Signature	
Date	17 March 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being forwarded to Examiner Lourdes Cruz via facsimile sent to 703-872-9318 on March 17, 2003.

Typed or printed name	Andrea R. Wolters		
Signature		Date	March 17 2003

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Group Art Unit	
Examiner Name	Lourdes C. Cruz
Total Number of Pages in This Submission	12
Attorney Docket Number	71522-2

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 130.00

Complete if Known	
Application Number	10/065,016 FAX RECEIVED
Filing Date	September 12, 2002
First Named Inventor	Olivier Boireau APR 0 8 2003
Examiner Name	Lourdes C. Cruz
Art Unit	TECHNOLOGY CENTER 2800
Attorney Docket No.	71522-2

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-2003

Deposit Account Name: McGarry Bair PC

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below	=	Fee Paid
Total Claims		- 20 =	0	x		=	$0
Independent Claims		- 3 =	0	x		=	$0
Multiple Dependent						=	$0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	130
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 130.00

SUBMITTED BY				(Complete *if applicable*)	
Name (Print/Type)	Joel E. Bair	*Registration No. (Attorney/Agent)*	33,356	*Telephone*	(616) 742-3500
Signature				*Date*	April 8, 2003

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Olivier Boireau

For: INTEGRATED CIRCUIT PACKAGE AND PRINTED CIRCUIT BOARD ARRANGEMENT

Serial No.: 10/065,016 Examiner: Lourdes C. Cruz

Filed: September 12, 2002 Group Art Unit: 2841

Atty. Docket: 71522-2 Confirmation No.: 5731

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

☐ deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents, Washington, DC 20231

☒ transmitted by facsimile to the Patent and Trademark Office, to Examiner Lourdes C. Cruz at 703-872-9318

Signature

Date: March 17 2003

Andrea R. Wolters
(type or print name of person certifying)

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Commissioner for Patents
Washington, D.C. 20231

Sir:

PETITION TO MAKE SPECIAL

Pursuant to 37 CFR §1.102(d), Applicant hereby petitions the Commissioner to make the above-referenced application, Serial No. 10/065,016, special for the reason that an infringing device is presently being made, offered for sale, sold, or used in the United States. This petition is accompanied by the requisite statement in support hereof, and the fee set forth in 37 CFR §1.17(h).

The references most closely related to the subject matter of the claims are U.S. Patent No. 4,994,902 to Okahashi et al. and U.S. Patent No. 5,923,540 to Asada et al. Copies are attached. The U.K. Patent Office cited these references during examination of the priority application in the U.K., which application has claims substantially similar in scope to those of the present application.

Okahashi '902 discloses a random set of pin locations (as illustrated in FIG. 6 and FIG. 7) for ground and power supply pins. There is no disclosure of inner portions and outer portions of an integrated circuit package. If it were to be interpreted by a person having ordinary skill in the art that the three rows and columns may be understood to comprise an outer portion, a middle portion and an inner portion, it is noted that one clock signal is located on an outer portion (outside row/column) and one clock signal located on a middle portion (of three rows/columns). The focus of Okahashi '902 is to link layers of multi-layer packages by arranging similar contacts/ pins to coincide vertically to higher layers, and is not remotely concerned with the difficulty in routing paths to/from the printed circuit board to the respective IC pins.

Okahashi '902 discloses a random distribution of power supply contacts, with (only by chance and not design) a minority of power supply contacts being located on an extremity of the IC. Thus, Okahashi '902 fails to disclose a majority of power supply contacts on an extremity of an integrated circuit package or printed circuit board. The feature of providing a majority of power supply contacts being located on an extremity in the present invention provides the advantage of enabling de-coupling capacitors to be located as close as possible to the power supply contacts. This minimizes track length and therefore resistance to the power supply contact, as described at paragraph 26 of the specification.

Furthermore, Okahashi '902 discloses one clock pin on an outer row/column and one clock pin on a middle row/column. However, it is noteworthy that the patent teaches, at col. 2 lines 44-45, that the clock signals can appear anywhere (so long as they are substantially matched on other 'vertical' layers for the co-processor!) But, regarding clock signals, one ordinarily skilled in the art is only taught by Okahashi '902 to surround clock signals by V_{ss} or V_{cc} fixed potential signals to keep them away from data (variable potential) signals. "This arrangement causes the fixed potential pins to shield electromagnetically the surroundings of the clock signal". Thus, Okahashi '902 fails to disclose a majority of clock contact points on an outer portion of an integrated circuit package or printed circuit board. The feature of providing a majority of clock contact points on an outer portion of an integrated circuit package or printed circuit board provides the advantage of enabling clock generation components to be located as close as

possible to the IC's clock contacts, as described at paragraph 25 of the specification. This minimizes track length, and therefore undesired parasitic capacitance and resistance, to the clock contact pins, as described at paragraph 27 of the specification.

Furthermore, Okahashi '902 discloses data contact points along one side of an IC, but specifically being arranged distal from the clock contact points. Thus, Okahashi '902 fails to disclose a majority of data contact points on an inner side of an outer portion of an integrated circuit package or printed circuit board. The feature of providing a majority of data contact points on an inner side of an outer portion of an integrated circuit package or printed circuit board provides the advantage of allowing relatively easy access in routing paths to/from the data points, as described at paragraph 35 of the specification.

Asada '540 discloses all power supply contacts randomly located on the outside of ground contact points. Indeed, the location of the power supply contact in FIG. 9B is the same as FIG. 1 (see col. 9 line 63 to col. 10 line 3) and is therefore NOT on the extremity. Thus, Asada '540 fails to disclose a majority of power supply contacts on an extremity of an integrated circuit package or printed circuit board. As mentioned above, the feature of providing a majority of power supply contacts being located on an extremity provides the advantage of enabling de-coupling capacitors to be located as close as possible to the power supply contacts. This minimizes track length and therefore resistance to the power supply contact, as described at paragraph 26 of the specification.

Furthermore, Asada '540 discloses nothing about specific locations of clock signal pins, save that pins generally can be located outside and/or inside a set of ground contact points. Thus, Asada '540 does not disclose a majority of clock contact points on an outer portion of an integrated circuit package or printed circuit board. The feature of providing a majority of clock contact points on an outer portion of an integrated circuit package or printed circuit board provides the advantage of enabling clock generation components to be located as close as possible to the IC's clock contacts, as described on page 13 line 23-29 of the specification. This minimizes track length, and therefore undesired parasitic capacitance and resistance, to the clock contact pins, as described at paragraph 25 of the specification.

Furthermore Asada '540 discloses nothing about specific locations of clock signal pins, save that the pins generally can be located outside and/or inside a set of ground

contact points. Thus, Asada '540 fails to disclose a majority of data signal contacts on an inner side of an outer portion of an integrated circuit package or printed circuit board. As mentioned above, the feature of providing a majority of data contact points on an inner side of an outer portion of an integrated circuit package or printed circuit board provides the advantage of allowing relatively easy access in routing paths to/from the data points, as described at paragraph 35 of the specification.

Respectfully submitted,
Olivier Boireau

Dated: 7 March 2003

By: _____

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